Title: Asymmetric Partially-Etched Leads for Finer Pitch Semiconductor Chip Package

ABSTRACT

A chip package having an array of leads, wherein successive leads are staggered in all three dimensions (X, Y, and Z) relative to one another. Such a staggered arrangement permits a large number of leads available in a confined space while maintaining the minimum separation necessary between adjacent leads. The leads are formed by placing asymmetric top and bottom masks on a lead frame, and partially etching the top of the lead frame, while partially and over etching the bottom of the lead frame. Although the resulting leads are staggered in three dimensions, no additional processing steps are needed beyond those used to fabricate conventional packages.